ELECTRICAL STRESS DE-RATING ANALYSIS

INTRODUCTION

The purpose of this document is to familiarize the user with the basic concepts of a de-rating analysis, starting with circuit analysis and proceeding through documentation. Electrical stress de-rating analysis is the process of determining a part's ability to withstand induced stresses under given environmental conditions. Induced stresses are taken from the datasheet and circuit analysis, and are identified in terms of voltage, current, power, etc. Environmental conditions refer primarily to temperature and are taken from the system's operating requirements.

One of the objectives of a stress analysis is to provide early warning of design deficiencies at the time in the program phase where changes are least expensive (i.e., while the design is still on paper). A stress analysis incorporated early into a program can significantly reduce test time and cost by providing a basis for a reliable design.

Transient conditions must also be taken into account. The analysis will not necessarily consider worst case conditions with regard to applied voltages or currents, part parameter values, or driving signals. However, when an undesirable stress condition is noted, worst case conditions should be examined and the probability of worst case occurrence investigated.

PRELIMINARY ANALYSIS

Prior to performing a stress de-rating analysis, a thermal analysis and circuit analysis must first be completed. Circuit analysis is considered outside the scope of this document. In brief, circuit analysis is the process used to calculate the electrical parameters of each part in the circuit, such as voltage, current, power, etc.

DETERMINING PART STRESS RATINGS

After thermal and electrical parameters are known, it is possible to calculate part stress ratings. The part stress rating is defined as the ratio of applied to rated electrical parameters. These electrical parameters may consist of voltage, current, power, inverse voltage, etc., or any combination, depending on the part. For example, a power stress ratio is used for a resistor, while a voltage stress ratio is used for a capacitor.

A part's stress rating can vary from lot to lot, vendor to vendor, application, and nearly always increases with increasing temperature. This document will concentrate on the latter; that is, how to calculate stress ratings with increasing temperatures. It will do this by presenting examples. For the purpose of these examples, it is assumed a thermal profile analysis has already been done in accordance with the Thermal Analysis document.

EXAMPLES

Example #1: Application of a Solid Tantalum Capacitor Voltage Rating

Given:

a. The device is a 6.8 μf electrolytic tantalum capacitor. Device ratings according to the datasheet are shown in Figure 1. Maximum rated operating voltage is 25 VDC up to 85°C. Absolute maximum operating temperature (T_{MAX}) is 125°C. The device is rated for operation up to 16 VDC of maximum operating at 125°C.

b. Maximum equipment external ambient temperature profile is 70°C. The internal temperature rise in the equipment was determined to be 30°C using the principles of the Thermal Analysis document.

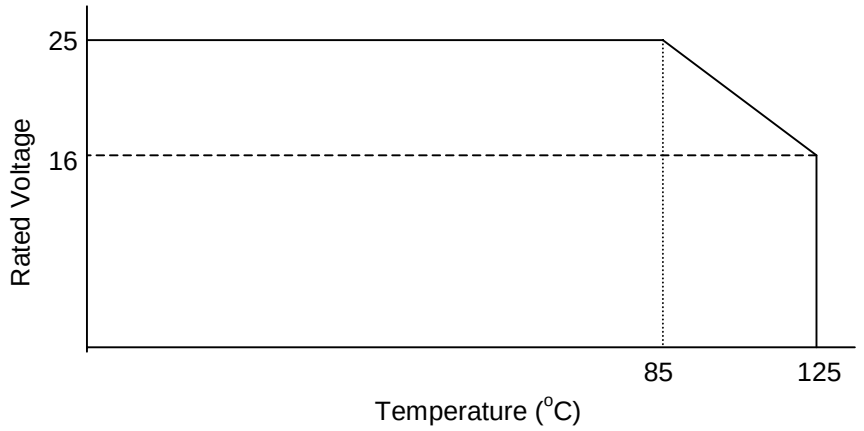

Figure 1: Maximum Voltage Rating for Electrolytic Tantalum Capacitor, Example # 1

c. Maximum impressed voltage is 10 VDC, determined from the electrical circuit analysis.

Determine:

a. The maximum voltage rating of the capacitor at the operating temperature.

b. The required capacitor voltage rating using the derating requirements in this manual.

Solution:

First, determine the part ambient operating temperature (T_{op}). This is the sum of the external ambient equipment temperature (70°C) and the internal temperature rise (30°C) or,

$$T_{op} = 70°C + 30°C = 100°C$$

At an operating temperature of 100°C, the maximum part rating is determined by one of formulas, depending on the operating temperature (T_{op}):

$$V_{MAX}(T_{OP}) = V_{MAX}(T_S) \qquad if\ T_{OP} < T_S$$

$$V_{MAX}(T_{OP}) = V_{MAX}(T_S) - \left(V_{MAX}(T_S) - V_{MAX}(T_{MAX})\right)\frac{T_{OP} - T_S}{T_{MAX} - T_S} \qquad if\ T_S < T_{OP} < T_{MAX} \quad \text{Eq-1}$$

$$V_{MAX}(T_{OP}) = 0 \qquad if\ T_{OP} > T_{MAX}$$

The operating temperature (T_{op}) given in the example (100°C) is between T_S (85°C) and T_{MAX} (125°C), so the center equation is used. Substituting:

$$V_{MAX}(100^O C) = V_{MAX}(85^O C) - \left(V_{MAX}(85^O C) - V_{MAX}(125^O C)\right)\frac{100^O C - 85^O C}{125^O C - 85^O C}$$

$$V_{MAX}(100^O C) = 25V - \left(25V - 16V\right)\frac{100^O C - 85^O C}{125^O C - 85^O C} = 21.6V$$

Or some users prefer to use the slope version of the formula instead, as follows, which yields identical results:

$$slope = \frac{rise}{run} = \frac{65\% - 100\%}{125^O C - 85^O C} = -0.00875/^O C$$

$$V_{MAX}(T_{OP}) = V_{MAX}(T_S)\left[1 - (slope)\left(T_S - T_{OP}\right)\right] \qquad \text{Eq-2}$$

$$V_{MAX}(100^O C) = V_{MAX}(85^O C)\left[1 + 0.00875/^O C\left(85^O C - 100^O C\right)\right]$$

$$V_{MAX}(100^O C) = 0.869\ V_{MAX}(85^O C) = (0.869)(25V) = 21.6V$$

For the solution to part (b) of the question, first determine the derating guidelines for tantalum capacitors. The derating guidelines for electrolytic tantalum capacitors 60% to T_S, and then linearly derated to T_{MAX} - 10°C. This is reproduced in Figure 2. Also shown is the operating temperature of the capacitor along with its maximum allowed stress ratio.

The maximum derated Stress Ratio (SR_D) at the operating temperature is calculated by the formula:

$$SR_D(T_{OP}) = SR_D(T_S) \qquad if\ T_{OP} < T_S$$

$$SR_D(T_{OP}) = SR_D(T_S) - (SR_D(T_S) - SR_D(T_D))\frac{T_{OP} - T_S}{T_D - T_S} \qquad if\ T_S < T_{OP} < T_{MAX} \qquad \text{Eq-3}$$

$$SR_D(T_{OP}) = 0 \qquad if\ T_{OP} > T_{MAX}$$

(Note this is identical to Eq-1 on the previous page except stress ratio is substituted for voltage.)

Substituting:

$$SR_{Derated}(100^O C) = 50\% - (50\% - 10\%)\frac{100^O C - 85^O C}{115^O C - 85^O C} = 30\%$$

The current 25V capacitor therefore does not meet the derating guidelines. The derated maximum rating is greater than the actual voltage the capacitor is expected to see, or:

$$Derated\ Max Voltage = (30\%)(25V) = 7.5V < 10V\ Actual$$

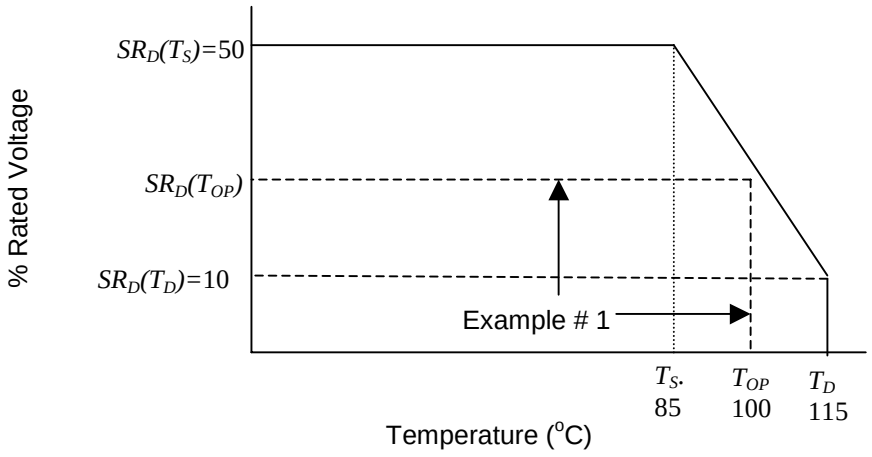

Figure 2: Derating Requirements For Electrolytic Tantalum Capacitor, Example # 1

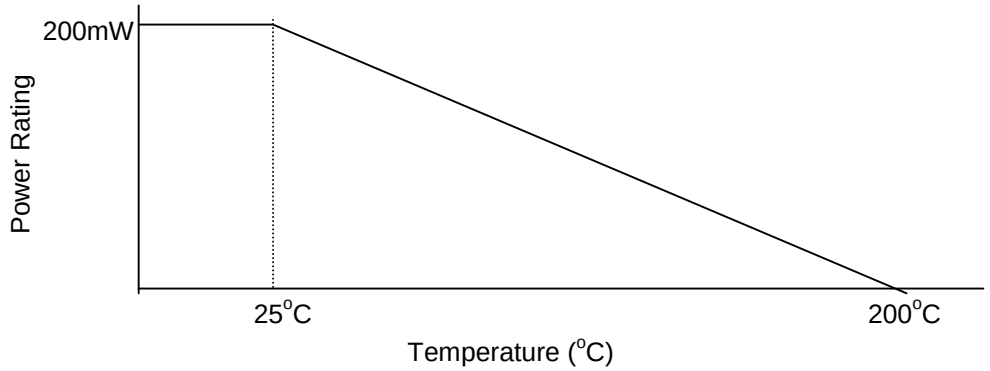

Figure 3: Maximum Power and Temperature Ratings Transistor, Example #2

To meet the derating guidelines, a capacitor with a voltage rating of at least 33.3 VDC is required, calculated as follows:

$$Min.Rating = \frac{V_{Nominal}}{SR_{Derated}} = \frac{10VDC}{30\%} = 33.3VDC$$

The proper capacitor is 6.8 µf, 35 VDC rated.

Example #2, Application of a Transistor

Given:

A user requires a transistor to be used in an application where it will be required dissipate 70 mW of power. Ambient temperature (T_A) in the immediate vicinity of the transistor is 50°C.

The selected transistor has maximum power dissipation ratings shown in Figure 3. The transistor can dissipate up to 200 mW at 25°C. Above 25°C, the datasheet requires the maximum power dissipation rating to be linearly "derated" to a maximum junction temperature (T_J) of 200°C. The transistor has a thermal resistance (Θ_{JA}) from junction to ambient of 0.875°C/mW.

Determine:

Determine if the selected resistor can be properly derated for the given application using the derating guidelines of this document.

Solution:

The derating guidelines for a silicon transistor are reproduced in Figure 4. T_S and T_{MAX} are taken from the datasheet and the given information. T_S is the maximum operating temperature at which full rated power can be applied, or in this case 25°C. T_{MAX} is the maximum junction temperature (T_J) or absolute maximum temperature at which the part can operate. In this case, it is 200°C. Maximum derated temperature (T_D) is then calculated by the formula:

$$T_D = T_S + 0.50(T_{MAX} - T_S)$$

Substituting,

$$T_D = 25^O C + 0.50(200^O C - 25^O C) = 112.5^O C \qquad \text{Eq-4}$$

The derating curve is now completely defined and shown in Figure 4.

Next, determine the derated stress ratio (SR_D) allowed by the derating guidelines. Equation # 3 is again used, except it is simplified because the derated stress ratio is zero at T_{MAX}, or

$$SR_D(T_{OP}) = SR_D(T_S) \qquad if\ T_{OP} < T_S$$

$$SR_D(T_{OP}) = SR_D(T_S)\left[1 - \frac{T_{OP} - T_S}{T_D - T_S}\right] \quad if\ T_S < T_{OP} < T_{MAX} \qquad \text{Eq-5}$$

$$SR_D(T_{OP}) = 0 \qquad if\ T_{OP} > T_{MAX}$$

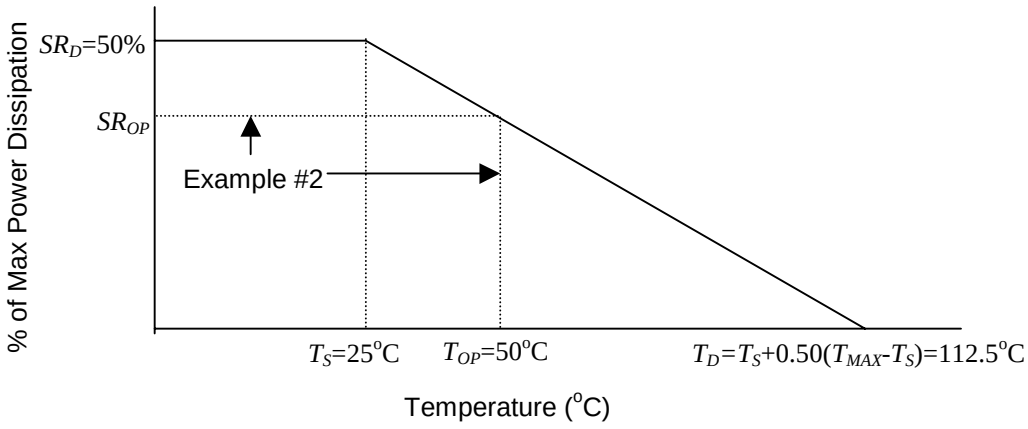

Figure 4: Transistor Derating Requirements, Example #2.

Operating temperature is 50°C. This is between T_{op} (25°C) and T_s (125°C), so the center equation is used. Substituting,

$$SR_D(95^O C) = SR_D(25^O C)\left[1 - \frac{50^O C - 25^O C}{112.5^O C - 25^O C}\right]$$

$$SR_D(95^O C) = 50\%\left[1 - \frac{50^O C - 25^O C}{112.5^O C - 25^O C}\right] = 35.7\%$$

The stress ratio allowed by the derating guidelines at an ambient temperature of 50°C is therefore 35.7% of the maximum power rating. Since the maximum power rating was given at 200 mW, the transistor is not allowed in an application where it dissipates more than 71.4 mW. Since its actual power dissipation was given at 70 mW, the transistor meets the derating guidelines.

Alternative Solution:

An alternate method of determining if the transistor exceeds its derating guidelines is to determine if actual junction temperature exceeds derated junction temperature.

Actual junction temperature is calculated using the thermal resistance properties of the device. The datasheet gave the thermal resistance, junction to ambient (Θ_{JA}), as 0.875°C/mW. We also know the transistor is dissipating 70mW of power. Junction temperature can therefore be calculated using the equation:

$$T_J = T_A + P\Theta_{JA}$$

Substituting:

$$T_J = 50^O C + (70mW)(0.875^O C / mW) = 111.25^O C$$

The derated junction temperature was previously calculated in Eq-4 to be 112.5°C. Since actual junction temperature does not exceed maximum derated junction temperature, the transistor is acceptable to use in the given application.

Note: the reason this short cut can be used is because the slope of the derating lines in both Figure 3 and Figure 4 is equal to the inverse of the thermal resistance. In other words, the junction temperature at any point along the derating line will be the same.

DOCUMENTING THE STRESS ANALYSIS

The next step in the electrical stress derating analysis process is to calculate the stress ratios and document the results of the stress analysis. The stress ratio is the numeric ratio between the actual stresses determined from the circuit analysis divided by the stress rating of the part at the operating temperature. This can be expressed mathematically as a percentage as follows:

The best method to document a stress analysis is usually through a worksheet or spreadsheet that allows for a logical flow of information from left to right with all required data and parameters specifically called out in columns. This obviates the casual omission of required parameters. The analysis is most effectively accomplished with the use of different worksheets for the various part categories. Many facilities perform the stress analysis, derating analysis, and reliability prediction all in a single spreadsheet to increase efficiency. It is also possible to generate macros to perform much of the repetitive work. Examples of typical worksheets are contained in the following pages containing Tables 1 through 6..

	Equipment	Schematic No. Rev Title:	Max Alt:
		Next Assy No. Title:	(ft)

Ref Des (type)	Const-Struction Resistive Element	Type	Vendor	Procur Doc	Nom Resist	Mfg Tol	T_A	Voltage		Power Dissipation			Percent Power Rated	Percent Voltage Rated	Wave Form (dc, sine, pulse, etc)	Remarks
								Nom Rated	Actual	Rated 25°C	Rated Max Amp	Actual				
					W	%	°C	V	V	mW	mW	mW	%	V		

Report Number	Rev Date	Proj Appd Date	Appd Date	Project No.	Sheet _____ of _____

Table 1: Part Usage and Applied Stress Data Chart for Resistors.

			Equipment				Schematic			No.		Rev			Max			
							Title:								Alt:			
							Next Assy			No.								
							Title:											(ft)
								Voltage										
								Rated		Operating								
Ref Des #	Const Dielec-tric	Cap Type	Vendor	Procur Doc	Part Amb Temp	Cap Value	Mfg Tol	25°C	T_D	DC	Peak	AC RMS	Freq	Pulse Peak	Rep Rate	% Volt Rating	Wave Form (dc, sine, pulse, etc)	Remarks
					°C	nF	%	V	V	VDC	V	V	KHz	V	ms	%		
Report Number				Rev		Date	Proj Appd		Date	Appd		Date	Project		No.	Sheet		
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Table 2: Part Usage and Applied Stress Data Chart for Capacitors.

		Equipment					Schematic Title:					No. Rev				Max Alt: (ft)									
							Next Assy Title:					No.													
Ref Des #	Vend Part #	Vend	Proc Doc	Type GP, Power, etc.	Part Amb Temp Nom Rated	Part Amb Temp Act	Contact Arrage-ment (form)	Contact Loading Con-tact	Power Nom Rated	Power Act	Current Rated	Current Act	Load res/ind cap	Coil Voltage Maximum Nom Rated	Maximum Act	Pickup Rated	Pickup Act	Dropout Nom Rated	Dropout Act	% Cont Power Rating	% Cont Curr Rating	% Coil Max Volt Rating	% Coil Pick Volt	% Coil Drop Volt
					°C	°C			mW	mW	mA	mA		mV	mV	mV	mV	mV	mV	%	%	%	%	%
Report Number				Rev		Date		Proj Appd		Date		Appd		Date		Project		No.		Sheet _____ of _____					

Table 3: Part Usage and Applied Stress Data Chart for Relays.

	Equipment	Schematic No. Rev Title: Next Assy No. Title:	Max Alt: (ft)

Ref Des #	Vendor Part #	Vendor	Procur Doc	Type Si Ge	Max Amb Temp	Voltage			Peak Inverse Voltage		Forward Current		Percent Current Rating	Percent PIV Rating	Θ	T_J	Notes
						Rated 25°C	Rated Max Ambient	Actual	Max Rated	Actual	Max Rated	Actual					
					°C	V	V	V	V	V	mA	mA	%	%	°C/W	°C	

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Table 4: Part Usage and Applied Stress Data Chart for Zener Diodes.

	Equipment	Schematic	No.	Rev	Max
		Title:			Alt:
		Next Assy	No.		
		Title:			(ft)

Ref Des #	Vendor Part #	Vendor	Procur Doc	Type Si Ge	Max Amb Temp	Power Dissipation			Peak Inverse Voltage		Forward Current		Percent Current Rating	Percent PIV Rating	Remarks
						Rated 25°C	Rated Max Ambient	Actual	Max Rated	Actual	Max Rated	Actual			
					°C	mW	mW	mW	V	V	A	A	%	%	

Report Number	Rev	Date	Proj Appd	Date	Appd	Date	Project	No.	Sheet
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Table 5: Part Usage and Applied Stress Chart for General Purpose and Power Rectifier Diodes.

			Equipment					Schematic Title:						No. Rev				Max Alt:			
								Next Assy Title:						No.				(ft)			
					Power Dissipation			Voltage						Current							
Ref Des #	Vend Part #	Vend	Proc Doc	Part Amb Temp	Rated @ 25°C	Rated @ T_D	Actual	Input Rated	Input Act	Output Rated	Output Act	Supply Rated	Supply Act	Collector Rated	Collector Act	Perc Input Rating	Perc Output Rating	Perc Supply Rating	Perc Current Rating	Perc I_C Rating	Q Res	T_J
				°C	mW	mW	mW	V	V	V	V	V	V	mA	mA	%	%	%	%	%	°C/W	(oC)
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Table 6: Part Usage and Applied Stress Data Chart for Linear Microcircuits.